10 GEA
10 Gigabit Ethernet Alliance

XAUI:
An Overview

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Authored by:
John D'Ambrosia, Tyco Electronics
Shawn Rogers, Texas Instruments
Jim Quilici, Intel Corporation

1300 Bristol Street North Suite 160 Newport Beach, Ca 92660 Tel: 949.250.7155 Fax: 949.250.7159 www.10gea.org

Executive Summary

The 10 Gigabit Attachment Unit Interface, "XAUI", is a technical innovation that dramatically improves and simplifies the routing of electrical interconnections. Developed by the IEEE 802.3ae 10 Gigabit Ethernet Task Force, XAUI delivers 10 Gb/s of data throughput using four differential signal pairs in each direction. Its compact nature and robust performance makes it ideal for chip-to-chip, board-to-board, and chip to optics module applications.

SERDES, ASIC, FPGA, and optical module vendors are all introducing products with XAUI interfaces. Industry efforts are underway as "plugfest" events are held to ensure that vendors' offerings are interoperable. The broad offering combined with on-going interoperability testing is driving XAUI to become the universal 10 Gb/s interface.

Introduction

This white paper is designed to provide a general overview of the XAUI interface (pronounced "zowie"), which is part of the impending 10 Gigabit Ethernet standard. Details of the technology are found in clauses 47 and 48 of the 10 Gb Ethernet standard (IEEE 802.3ae), which is currently on track for IEEE approval by mid-2002.

This paper is sponsored by the 10 Gigabit Ethernet Alliance – a group of companies interested in promoting the forthcoming standard. This paper describes XAUI's role in the 10 Gigabit Ethernet architecture and provides a description of its basic operation.

Architecture

Under the International Standards Organization's Open Systems Interconnection (OSI) model, Ethernet is fundamentally a Layer 2 protocol. An Ethernet PHYsical layer device (PHY), which corresponds to Layer 1 of the OSI model, connects the media (optical or copper) to the MAC layer, which corresponds to OSI Layer 2.

The 802.3ae specification defines two PHY types: the LAN PHY and the WAN PHY. The WAN PHY has an extended feature set added onto the functions of a LAN PHY. Ethernet architecture further divides the PHY (Layer 1) into a Physical Media Dependent (PMD) and a Physical Coding Sublayer (PCS). The two types of PHYs are solely distinguished by the PCS. Figure 1 gives a graphical overview of the architectural components of the LAN / WAN PHY.

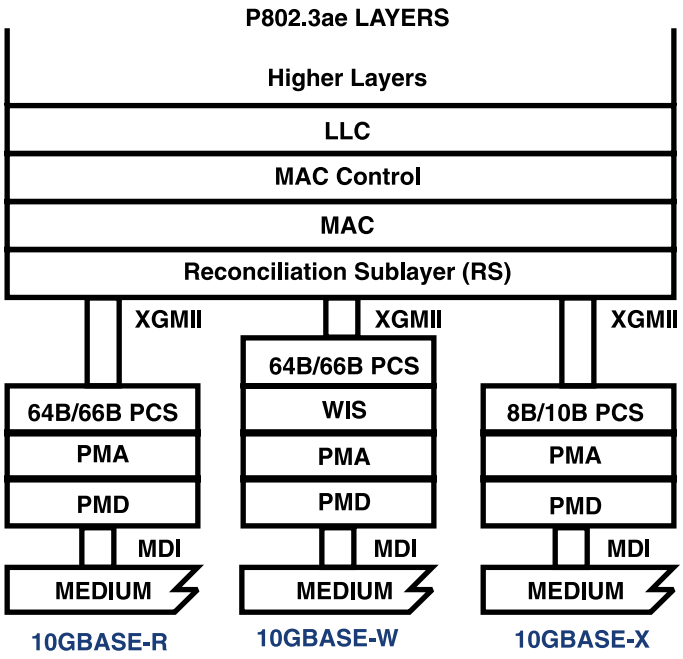

Figure 1: Architectural Componenets of the LAN/WAN/PHY

Between the MAC and the PHY is the XGMII, or 10 Gigabit Media Independent Interface. The XGMII provides full duplex operation at a rate of 10 Gb/s between the MAC and PHY. Each direction is independent and contains a 32-bit data path, as well as clock and control signals. In total the interface is 74 bits wide.

While XGMII provides a 10 Gb/s pipeline, the separate transmission of clock and data coupled with the timing requirement to latch data on both the rising and falling edges of the clock results in significant challenge in routing the bus more than the recommended short distance of 7 cm. For this reason, chip-to-chip, board-to-board and chip-to-optical module applications are not practical with this interface. Consequently, the XGMII bus puts many limitations on the number of ports that may be implemented on a system line card.

Architecture (Continued)

To overcome these issues, the 10 Gigabit Ethernet Task Force developed the XAUI interface. XAUI is a full duplex interface that uses four (4) self-clocked serial differential links in each direction to achieve 10 Gb/s data throughput. Each serial link operates at 3.125 Gb/s to accommodate both data and the overhead associated with 8B/10B coding. The self-clocked nature eliminates skew concerns between clock and data, and extends the functional reach of the XGMII by approximately another 50 cm. Conversion between the XGMII and XAUI interfaces occurs at the XGXS (XAUI Extender Sublayer).

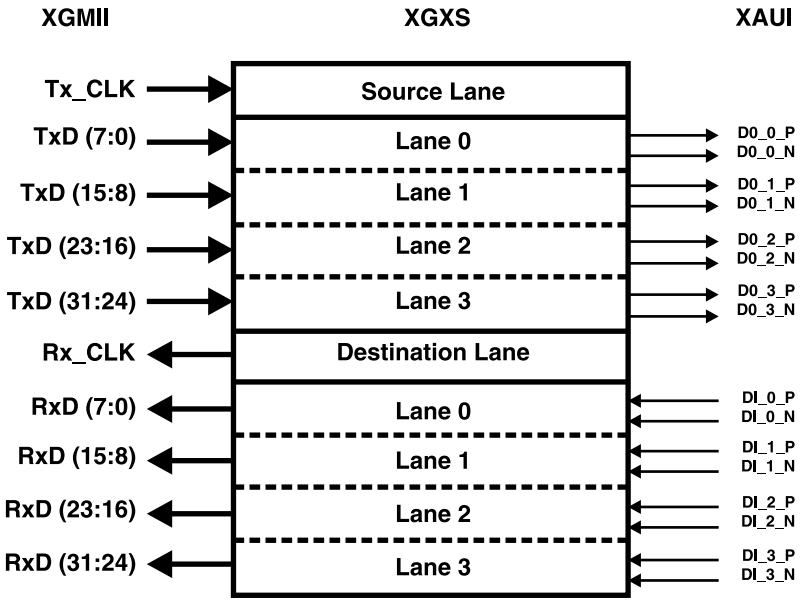

Figure 2: XGMII to XAUI at the XGXS

As seen in Figure 2, the XGMII interface is organized into 4 lanes of 8 bits. At the source side of the XAUI interface bytes on a given lane as well as the timing clock are converted within the XGXS into an 8B / 10B encoded data stream. Each data stream is transmitted across a single differential pair running at 3.125 Gb/s. At the destination side of the interconnect the clock is recovered from the incoming data stream, it is decoded and then mapped back to the 32 bit XGMII format. . Thus, the 74 pin wide XGMII interface is reduced to a XAUI interface consisting of 8 differential pair or 16 pins. Furthermore, the source synchronous clocking scheme allows XAUI to cross clock domains, which eliminates elaborate timing correction within the system.

A Self-Managed Interface

The XAUI employs the same robust 8B/10B transmission code as 1000BASE-X. With 8b/10b coding, there are more than enough code possibilities for mapping an 8-bit word. Some of the extra code groups are used for control signaling; such as start of frame, end of frame, channel idle, link configurations and so on. Control words are used during the Inter-Packet Gap (IPG) time and during idle periods to continuously allow the interface to maintain word and lane allignment. This is done with no upper layer support requirement, and allows XAUI to function as a self-managed interface.

Frame synchronization and lane alignment is essentially a two-step process. Code group synchronization is achieved on each lane upon reception of three ordered sets for the lane. One easily recognizable patterns called comma /K/ enables the XAUI receiver to attain frame alignment on the incoming bit stream. Each lane adjusts for proper alignment to the /K/ whenever it appears. However, each serial transmission lane operates independently and can often come out of alignment with respect to one another. As shown in Figure 3, lane alignment is accomplished by use of a control word defined for alignment, referred to as /A/. The XAUI line protocol defines specific times during the IPG when an /A/ word should be passed on all four lanes simultaneously. The receiving connection uses these words to correct for lane-to-lane skew common in most connections. The XAUI interface can lane align with up to 40bits (12.8ns) of skew between lanes, allowing for significant flexibility in board design.

Figure 3: Lane Alignment

Furthermore, XAUI compensates for differences in clock domains that often exist between each side of the link. By monitoring the difference between incoming and outgoing data rates, each XAUI connection can add or delete specific control words in the IPG, referred to as /R/ to balance the data rate at each connection without effecting lane disparity.

Interoperability

The 10 Gigabit Ethernet Alliance formed a working group to examine interoperability between different vendors' XAUI implementation. This group worked in conjunction with the 10 Gigabit Ethernet Consortium to define the test methodology and environment under which interoperability testing would be performed. The 10 Gigabit Ethernet Consortium, which will be responsible for performing interoperability testing between different vendors' XAUI implementation, has adopted the work completed by this group.

Multiple vendors have demonstrated XAUI interoperability. All devices tested were designed to the IEEE 802.3ae specification. Each vendor has demonstrated bit error rates of 10^{-12} over PC board traces of 50 cm length, demonstrating the robustness of the technology and completeness of the standard. The basic nature of XAUI enables it to be scaleable, which will provide users with a future upgrade path to extend the life of their systems.

For more information on XAUI Interoperability testing, please visit the 10 Gigabit Ethernet Consortium at http://www.iol.unh.edu/consortiums/10gec.

XAUI - The Universal Interface

The 10 Gigabit Attachment Unit Interface, "XAUI", is a technical innovation that dramatically improves and simplifies the routing of electrical interconnections. It helps to overcome the length limitation associated with the XGMII, which provides full duplex operation at a rate of 10 Gb/s between the Ethernet MAC and PHY layers. By extending the physical separation between the MAC and PHY, the interface allows for fan-out on multi-port line cards or connections to other cards within the system chassis. In addition, the self-managed interface helps to overcome associated clocking issues, which leads to a more easily implemented solution.

SERDES, ASIC, FPGA, and optical module vendors are all introducing products with XAUI interfaces. For example, XAUI has been selected as the interface for 10G Ethernet Z-Axis Pluggable Module MSA's (Multi-Source Agreements), such as XGP and XENPAK. Broad product support for combined with its ease of use is driving XAUI to become the universal 10Gb/s interface.